IN THE CLAIMS

What is claimed is:

1. A semiconductor device including an insulated gate field effect transistor (IGFET), comprising:

a gate electrode of the IGFET having a lower layer electrode formed on a gate insulating film and an upper layer electrode formed on the lower layer electrode;

a cap film formed on the upper layer electrode;

a first nitride film on a side surface of the upper layer electrode;

an oxide film on a side surface of the lower layer electrode; and

an etching stopper film including a second nitride film formed on the outside of the first nitride film and oxide film.

2. The semiconductor device according to claim 1, wherein:

first nitride film is a thermal nitride film.

3. The semiconductor device of claim 2, wherein:

first nitride film is a rapidly heated thermal nitride film.

4. The semiconductor device of claim 2, wherein:

the first nitride film has a film thickness of approximately 2 to 5 nm.

5. The semiconductor device of claim 2, further including:

an interlayer insulating film formed to cover the gate electrode of the IGFET;

a contact hole opened in the interlayer insulating film to expose a source/drain region of the IGFET; and

a conductor filling the contact hole and electrically connected with the source/drain region.

6. The semiconductor device of claim 2, wherein:

the oxide film is a thermal oxide film.

7. The semiconductor device of claim 2, wherein:

the second nitride film is formed with chemical vapor deposition (CVD).

8. A method for manufacturing a semiconductor device including an insulated gate field effect transistor (IGFET), comprising the steps of:

forming a gate insulating film on a semiconductor substrate;

forming a laminate film on the gate insulating film, the laminate film including an insulating film formed on a second conductive film formed on a first conductive film;

etching the insulating film and second conductive film into a predetermined pattern to form a cap film and an upper layer gate electrode;

forming a first nitride film on the side surface of the upper layer gate electrode;

etching the first conductive film using the cap layer, upper layer gate electrode, and the nitride film as a mask to form a lower layer gate electrode;

forming a first oxide film on the side surface of the lower layer electrode; and

forming an etching stopper film including a second nitride film over the entire surface.

9. The method for manufacturing a semiconductor device of claim 8, wherein:

the first conductive film includes a polysilicon film; and

the second conductive film includes a metal film.

10. The method for manufacturing a semiconductor device of claim 8, wherein:

the first conductive film includes a polysilicon film; and

the second conductive film includes a metal silicide film having a high melting point.

11. The method for manufacturing a semiconductor device of claim 8, wherein

the first nitride film is a thermal nitride film; and

the first oxide film is a thermal oxide film.

12. The method for manufacturing a semiconductor device of claim 8, wherein:

forming the etching stopper film includes forming the second nitride film with a chemical vapor deposition.

13. The method for manufacturing a semiconductor device of claim 8, wherein:

the first nitride film is a thermal nitride film formed with a rapid thermal nitridation step using a lamp as a heat source.

14. The method for manufacturing a semiconductor device of claim 8, further including the steps of:

forming a source/drain region by doping an impurity into the semiconductor substrate after the step of forming the first oxide film; and

forming an interlayer insulating film over the entire surface and selectively etching the interlayer insulating film with a selective etching ratio for the etching stopper film to open a contact hole after the step of forming the etching stopper film.

15. The method for manufacturing a semiconductor device of claim 8, further including the steps of:

forming a LDD (lightly doped drain) region by doping a first impurity concentration into the semiconductor substrate after the step of forming the first oxide film;

anisotropic etching the etching stopper film to form a side wall etching stopper film on side surfaces of the lower layer gate electrode, upper layer

gate electrode and cap layer; and

forming a source/drain region by doping a second impurity concentration into the semiconductor substrate using the side wall etching stopper film as a mask wherein the first impurity concentration is lower than the second impurity concentration.

16. The method for manufacturing a semiconductor device of claim 15, further including the steps of:

forming a second oxide film over the entire surface of the substrate with a chemical vapor deposition method;

anisotropic etching the second oxide film to form a side oxide film on the side surface of the etching stopper film; and

forming the source/drain region after the step of forming the side wall.

17. A semiconductor device including a first region and a second region, comprising:

a first gate electrode of a first IGFET in the first region having a first lower layer electrode formed on a first gate insulating film and a first upper layer electrode formed on the first lower layer electrode;

a first cap film formed on the first upper layer electrode;

a first nitride film on a side surface of the first upper layer electrode;

a first oxide film on a side surface of the first lower layer electrode;

a first etching stopper film including a second nitride film formed on the outside of the first nitride film and first oxide film;

a second gate electrode of a second IGFET in the second region having a second lower layer electrode formed on a second gate insulating film and a second upper layer electrode formed on the second lower layer electrode;

a second cap film formed on the second upper layer electrode;

a third nitride film on a side surface of the second upper layer electrode;

a second oxide film on a side surface of the second lower layer electrode;

a second etching stopper film including a fourth nitride film formed on the outside of the third nitride film and second oxide film; and

wherein the first IGFET includes a lightly doped drain.

18. The semiconductor device of claim 17, wherein:

the semiconductor device is a semiconductor memory device.

19. The semiconductor device of claim 18, wherein:

the first region is a memory cell region and the second region is a peripheral circuit region.

20. The semiconductor device of claim 19, further including:

a first contact providing an electrical connection to a first source/drain region of the first IGFET;

a second contact providing an electrical connection to a second

source/drain region of the second IGFET; and

a first spacing from the first contact to the first gate electrode is greater than a second spacing from the second contact to the second gate electrode.